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 COPYRIGHT AND RELATED  
 INTELLECTUAL PROPERTY LAW

September 23, 2004

Mail Stop Certificate of Corrections Branch  
 Commissioner for Patents  
 P.O. Box 1450  
 Alexandria, VA 22313-1450

Re: U.S. Patent No.: 6,787,876  
 Issued: September 7, 2004  
 Inventor: Martin Clive Wilson  
 Our Docket: 33908

**Certificate  
 OCT 04 2004  
 of Correction**

Sir:

A Certificate of Correction under 35 U.S.C. 254 is hereby requested to correct Patent Office printing errors in the above-identified patent. Enclosed herewith is a proposed Certificate of Correction (Form No. PTO-1050) for consideration along with appropriate documentation supporting the request for correction.

It is requested that the Certificate of Correction be completed and mailed at an early date to the undersigned attorney of record. The proposed corrections are obvious ones and do not in any way change the sense of the application.

We understand that a check is not required since the errors were on the part of the Patent and Trademark Office in printing the patent.

Very truly yours,

Jeffrey J. Sopko, Reg. No. 27676

JJS:vln  
 Enclosures

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

Jeffrey J. Sopko

Name of Attorney for Applicant(s)

September 23, 2004

Date

Signature of Attorney

OCT 05 2004

**UNITED STATES PATENT AND TRADEMARK OFFICE**  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,787,876 B2 PAGE 1 OF 1  
DATED : September 7, 2004  
INVENTOR(S) : Martin Clive Wilson

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

**Column 4**

Line 43, after "from" please delete "1" and insert therefor - - 3 - -.

MAILING ADDRESS OF SENDER:

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PATENT NO. 6,787,876 B2

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⇒ 0

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1           **Claim 3 (Original):** A semiconductor device is  
2         claimed in claim 2, wherein said distance lies within the  
3         range of from 3  $\mu\text{m}$  to 5  $\mu\text{m}$ .

1           **Claim 4 (Original):** A semiconductor device as  
2         claimed in any one of claims 1 to 3, wherein there are two  
3         trenches, each of which has the features defined in  
4         claim 1, and wherein an active device is formed in the  
5         semiconductor material layer between the two trenches.

1           **Claim 5 (Currently amended):** A semiconductor device  
2         as claimed in any one of claims 1 to [[4]] 3, wherein there  
3         are a plurality of trenches, each of which has the features  
4         defined in claim 1, and wherein a respective active device  
5         is formed in the semiconductor material layer between each  
6         pair of adjacent trenches.

1           **Claim 6 (Currently amended):** A semiconductor device  
2         as claimed in any one of claims 1 to [[5]] 3, wherein the  
3         semiconductor material layer is a silicon layer.

1           **Claim 7 (Original):** A semiconductor device as  
2         claimed in claim 6, wherein the silicon layer is of single  
3         crystal formation.